WHAT IS CLAIMED IS:

1. A cell processing method in an asynchronous transfer mode (ATM) switch comprising:

storing unicast cells and multicast cells in a buffer, and storing addresses of the respective cells in address queues;

assigning respective priorities to the cells stored in the buffer;

reading out the cells from the buffer according to the assigned priorities; and

sending the cells read out from the buffer to fan-out ports, and determining a selected cell for output.

2. The cell processing method of claim 1, wherein the addresses stored in the address queues are addresses of the cells stored in the buffer.

3. The cell processing method of claim 1, wherein the multicast cell addresses are stored in the address queues separate from the unicast cell addresses.

4. The cell processing method of claim 1, wherein the address queues for storing the multicast cell addresses are multicast connection identifier (MCI) address queues maintained for each MCI.

5. The cell processing method of claim 4, wherein the MCI address queue has one write pointer and a plurality of read pointers equal in number to multiple fan-out ports.

6. The cell processing method of claim 1, wherein the buffer is a shared buffer memory.

7. The cell processing method of claim 1, wherein the priorities of the unicast cells are determined by an order of respective input to the address queues.

8. The cell processing method of claim 1, wherein the assigning the priorities comprises:

calculating queue lengths for the respective fan-out ports;

determining the priorities by comparing the calculated queue lengths for the respective fan-out ports; and

confirming a location where buffers having the cells with the determined priorities are stored.

9. The cell processing method of claim 8, wherein the queue lengths are equal to a respective difference value between a write pointer address and each of a plurality of the read pointer addresses corresponding to a fan-out port.

10. The cell processing method of claim 1, wherein when a head of line (HOL) blocking occurs between the unicast cells during the reading out the cells from the buffer, the unicast cell having a higher priority is read out first, wherein when the HOL blocking occurs between the multicast cells during the reading out the cells from the buffer, the multicast cell having a higher priority is read out first, and wherein when the HOL blocking occurs between the unicast cell and the multicast cell during the reading out the cells from the buffer, the unicast cell is first read out first.

11. The cell processing method of claim 1, wherein the determining the selected cell for output at the fan-out ports comprises outputting the cell having a longer queue length as the selected cell when the unicast cell and the multicast cell simultaneously reach the fan-out port.

12. The cell processing method of claim 1, wherein the reading out the cells from the buffer is performed three times for one slot time.

13. A cell processing method in an asynchronous transfer mode (ATM) switch comprising:

storing unicast cells and multicast cells in a buffer, and storing addresses of the respective cells in address queues;

calculating queue lengths for respective fan-out ports of the address queues;

determining priorities of the cells by comparing the calculated queue lengths;

confirming storage locations of the cells having the determined priorities in the buffer;

reading out the cells from the buffer according to the determined priorities; and

sending the cells read out from the buffer to the fan-out ports and determining a cell of the sent cells to a fan-out port for output.

14. The cell processing method of claim 13, wherein the addresses stored in the address queues are addresses of the cells stored in the buffer.

15. The cell processing method of claim 13, wherein the multicast cell addresses are stored in multicast address queues and the unicast cell addresses are stored in unicast address queues.

16. The cell processing method of claim 13, wherein the address queues for storing the multicast cell addresses are multicast connection identifier (MCI) address queues maintained for each MCI.

17. The cell processing method of claim 16, wherein each MCI address queue has one write pointer and read pointers equal in number to fan-out ports.

18. The cell processing method of claim 13, wherein the buffer is a shared buffer memory.

19. The cell processing method of claim 13, wherein the priorities of the unicast cells are determined according to sequential input to the address queues.

20. The cell processing method of claim 13, wherein the queue length is a difference value between a write pointer address and a read pointer address.

21. The cell processing method of claim 13, wherein when a head of line (HOL) blocking occurs between the unicast cells during the reading out the cells from the buffer, the unicast cell having a higher priority is read out first, wherein when the HOL blocking occurs between the multicast cells during the reading out the cells from the buffer, the

multicast cell having a higher priority is read out first, and wherein when the HOL blocking occurs between the unicast cell and the multicast cell during the reading out the cells from the buffer, the unicast cell is read out first.

22. The cell processing method of claim 13, wherein of the sent cells, cells that reach a prescribed fan-out port are one of only a unicast cell, only a multicast cell and both the unicast cell and the multicast cell concurrently, and wherein when both the unicast cell and the multicast cell reach concurrently, the cell having a longer queue length is output.

23. A cell processing apparatus in an asynchronous transfer mode (ATM) switch comprising:

a buffer that stores cells inputted to the ATM switch;

multicast connection identifier (MCI) address queues that store buffer addresses of multicast cells;

unicast address queues that store buffer addresses of unicast cells; and

fan-out ports that receive the cells from the respective address queues, and output the received cells to corresponding destinations.

24. The cell processing apparatus of claim 23, wherein the MCI address queue has one write pointer and read pointers equal in number to the fan-out ports.

25. The cell processing apparatus of claim 23, wherein the buffer is a shared buffer memory.

26. The cell processing apparatus of claim 23, wherein the ATM switch first reads out a unicast cell having a higher priority when head of line (HOL) blocking is produced between the unicast cells, wherein the ATM switch first reads out a multicast cell having a higher priority when the HOL blocking is produced between the multicast cells, and wherein the ATM switch first reads out the unicast cell irrespective of the queue length of the cells when the HOL blocking is produced between the unicast cell and the multicast cell.

27. The cell processing apparatus of claim 23, wherein the ATM switch reads the shared buffer memory three times for one cell time slot.

28. The cell processing apparatus of claim 23, wherein the ATM switch determines the cell to be outputted according to the queue length when a multicast cell and a unicast cell concurrently reach a fan-out port.